



Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

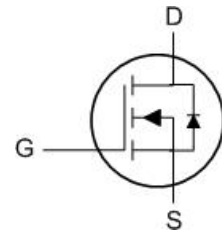
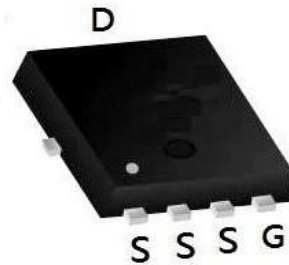
Product Summary

BVDSS	RDSON	ID
30V	2.0mΩ	120A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN5060-8L(CLIP) Pin Configuration



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$	I_D	120	A
	$T_C=100^{\circ}\text{C}$		75	
Pulsed Drain Current ¹		I_{DM}	380	A
Single Pulse Avalanche Energy ²		E_{AS}	101	mJ
Total Power Dissipation	$T_C=25^{\circ}\text{C}$	P_D	69	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	50	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.8	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30	-	-	V
Gate-body Leakage Current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	-	-	1	μA
	T _J =125°C			-	2	-	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.3	-	2.3	V
Drain-Source On-Resistance ⁴		R _{DS(on)}	V _{GS} = 10V, I _D = 22.5A	-	2.0	2.4	mΩ
			V _{GS} = 4.5V, I _D =22.5A	-	3.0	3.8	
Forward Transconductance ⁴		g _{fs}	V _{DS} = 10V, I _D = 20A	-	130	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = 15V, V _{GS} =0V, f =1MHz	-	2566	-	pF
Output Capacitance		C _{oss}		-	1419	-	
Reverse Transfer Capacitance		C _{rss}		-	111	-	
Gate Resistance		R _g	f = 1MHz	-	2.5	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = 10V, V _{DS} = 15V, I _D = 20A	-	39	-	nC
Gate-Source Charge		Q _{gs}		-	11	-	
Gate-Drain Charge		Q _{gd}		-	4.5	-	
Turn-On Delay Time		t _{d(on)}	V _{GS} =10V, V _{DD} = 20V, R _G = 3Ω, I _D = 20A	-	10	-	ns
Rise Time		t _r		-	37	-	
Turn-Off Delay Time		t _{d(off)}		-	45	-	
Fall Time		t _f		-	16	-	
Body Diode Reverse Recovery Time		t _{rr}	I _F =20A, dI/dt=100A/μs	-	49	-	ns
Body Diode Reverse Recovery Charge		Q _{rr}		-	35	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = 45, V _{GS} = 0V	-	-	1.4	V
Continuous Source Current	T _C =25°C	I _S	-	-	-	120	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = 24V, V_{GS} = 10V, L = 0.1mH, R_g = 25\Omega$
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

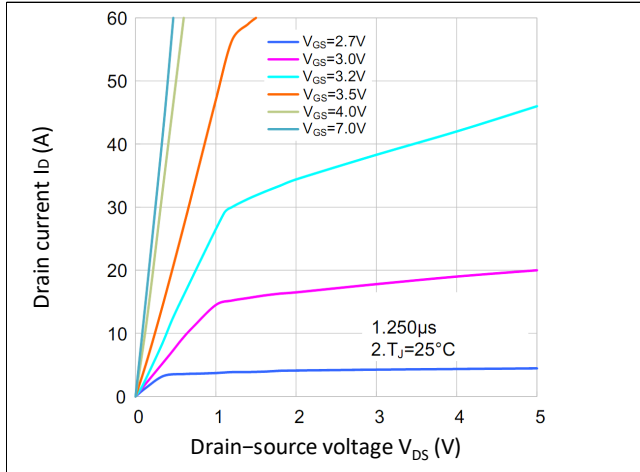


Figure 1. Output Characteristics

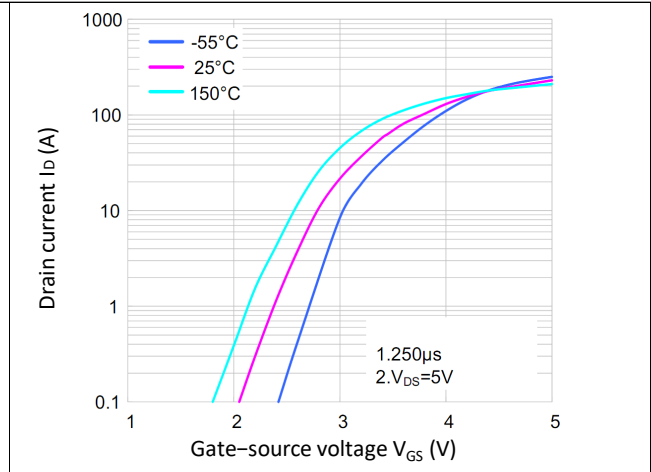


Figure 2. Transfer Characteristics

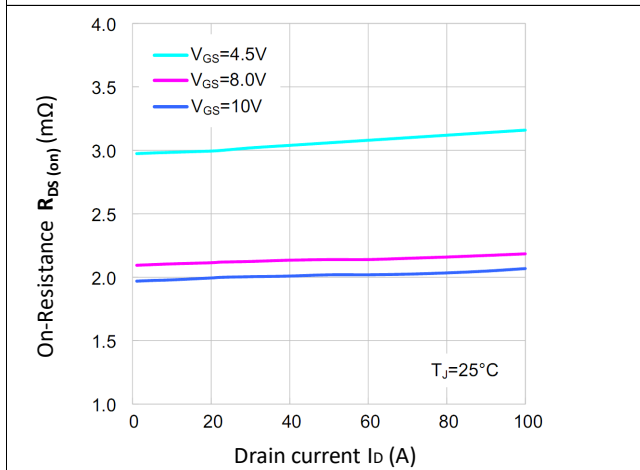


Figure 3. $R_{DS(ON)}$ vs. I_D

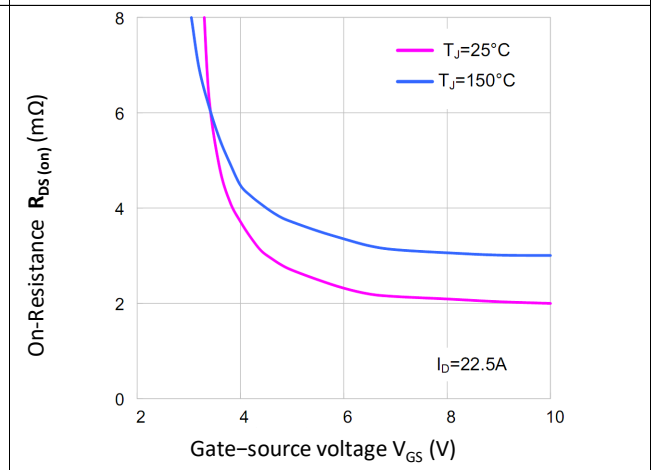


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

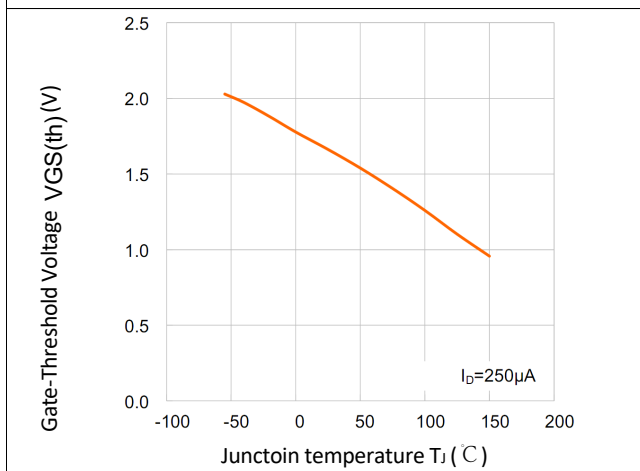


Figure 5. $V_{GS(th)}$ vs. T_J

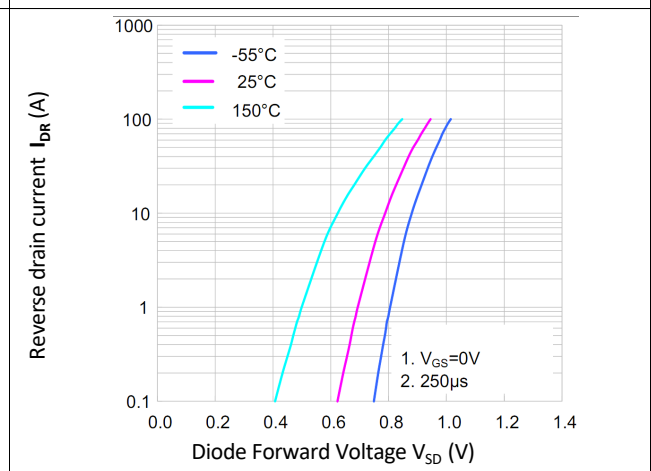


Figure 6. I_{DR} vs. V_{SD}

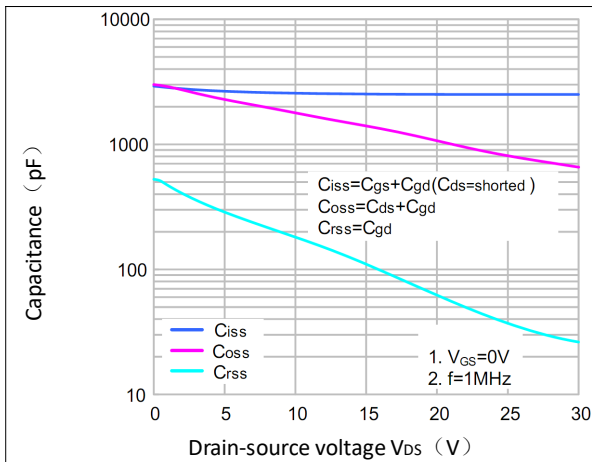


Figure 7. Capacitance Characteristics

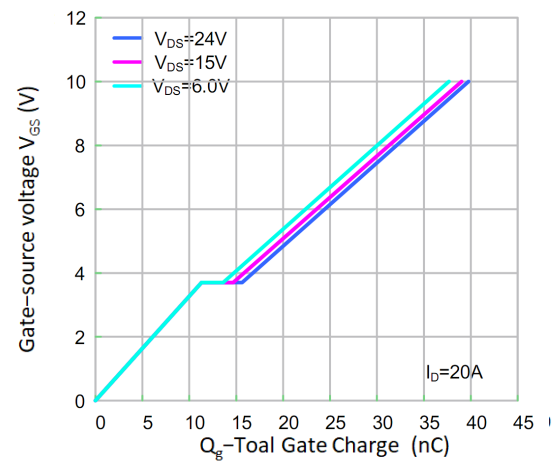


Figure 8 Gate Charge Characteristics

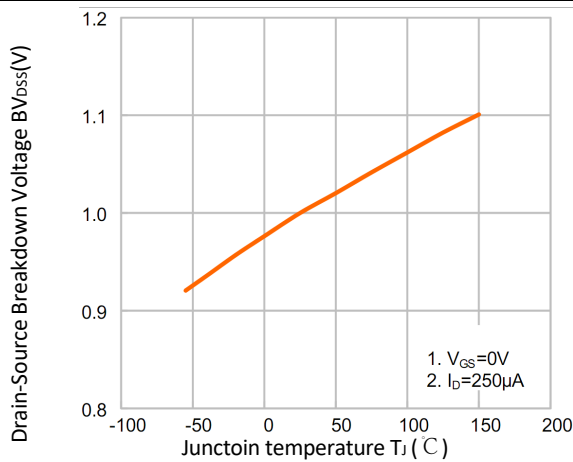


Figure 9. BV_{DSS} VS T_J

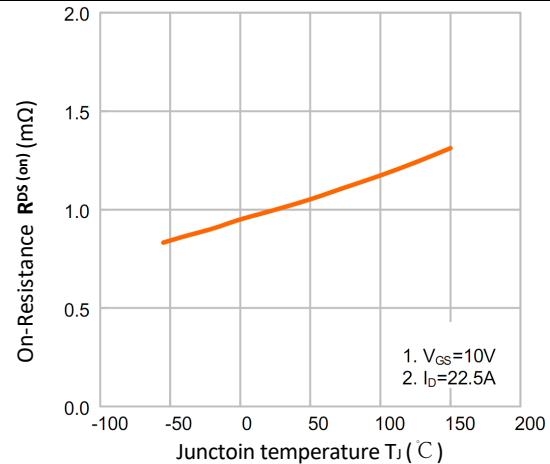


Figure 10. R_{DS(ON)} VS T_J

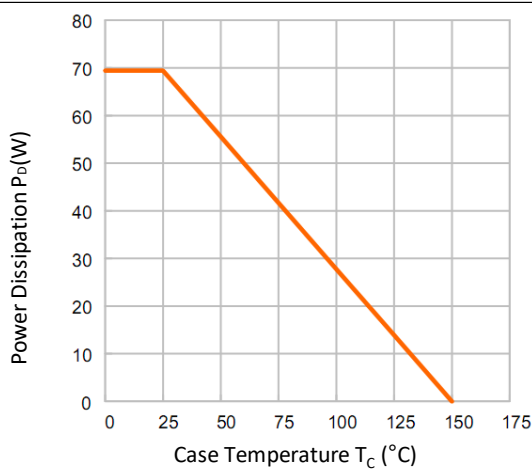


Figure 11. Power Dissipation

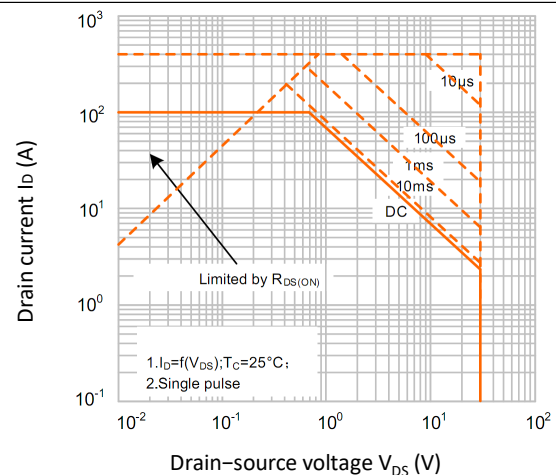


Figure 12. Safe Operating Area

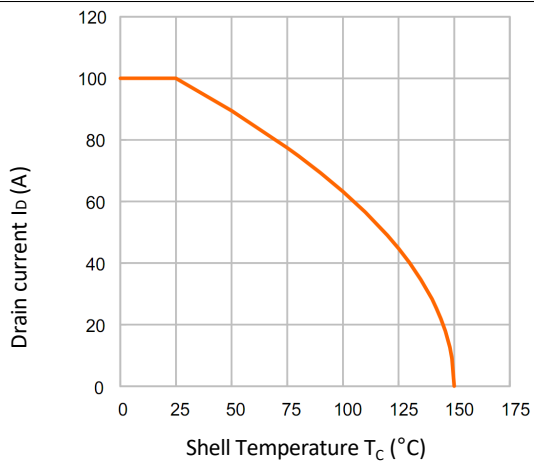


Figure 13.Drain current VS Shell Temperature

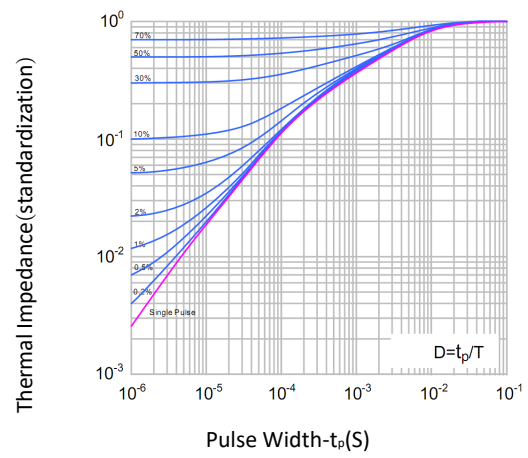


Figure 14 Transient thermal impedance VS Pulse Width



Test Circuit

PDFN5060-8L Package Information

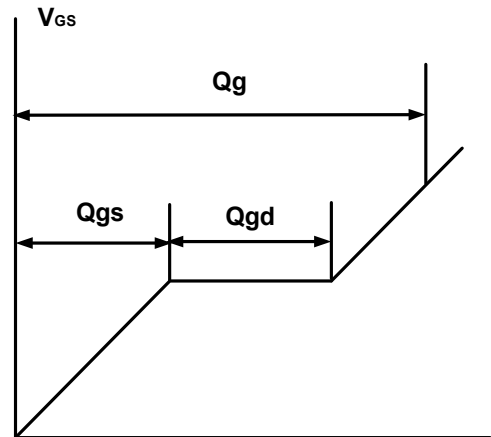
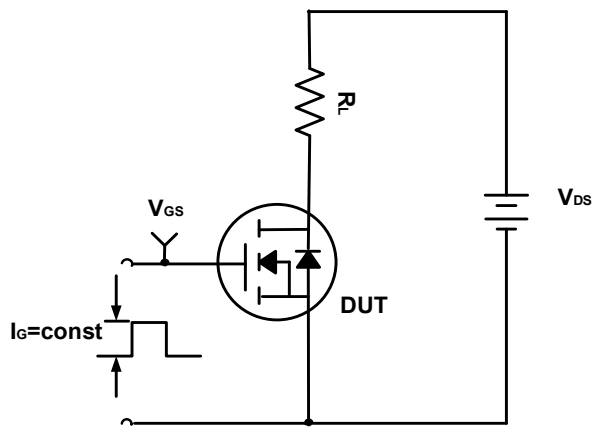


Figure A. Gate Charge Test Circuit & Waveforms

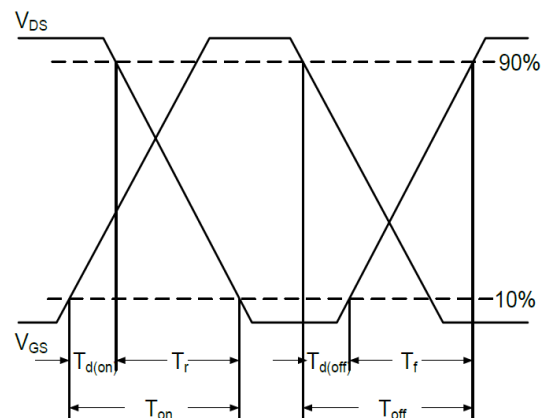
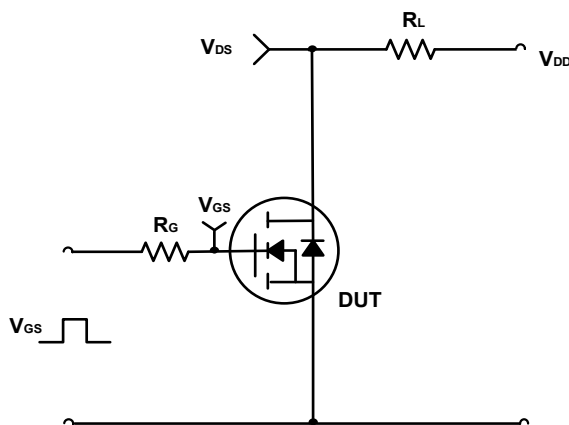
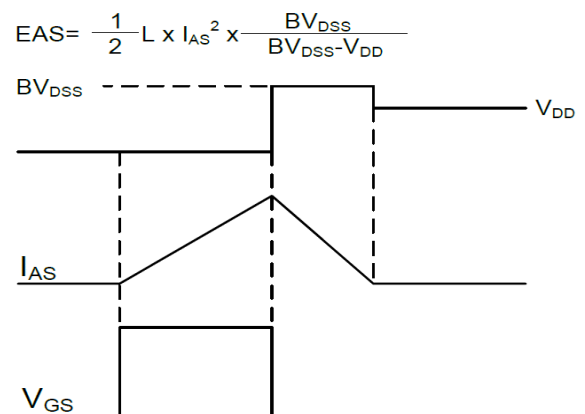
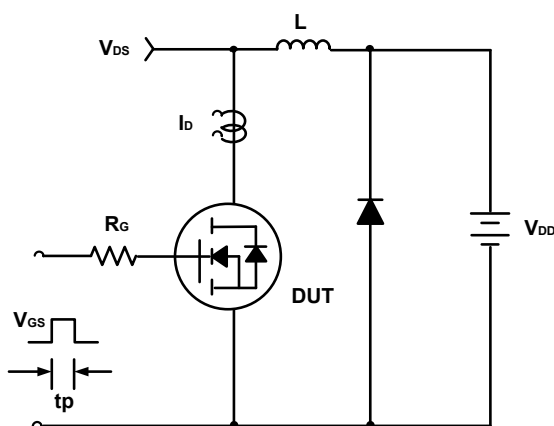


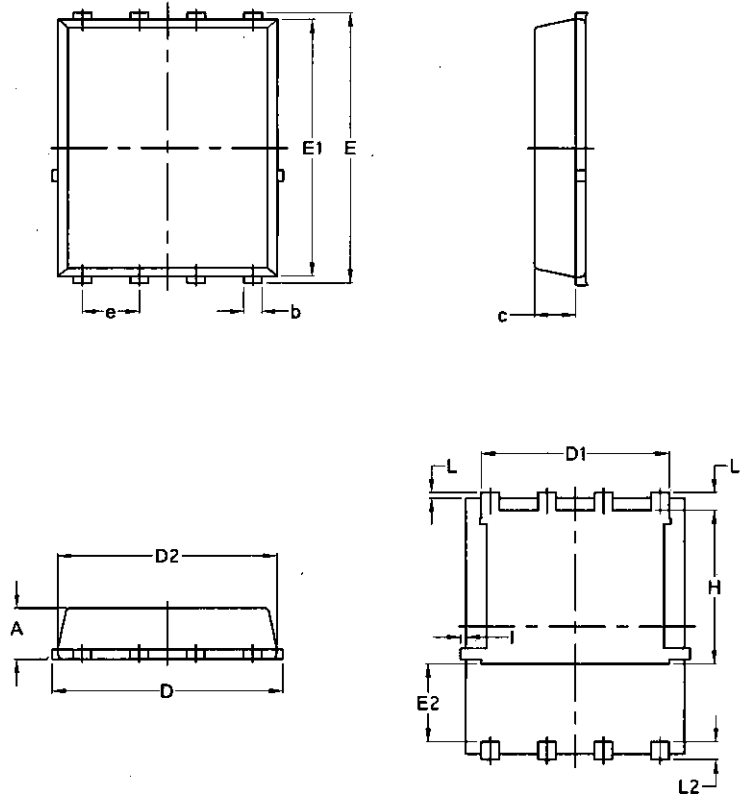
Figure B. Switching Test Circuit & Waveforms



$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DS}}{BV_{DS} - V_{DD}}$$

Figure C. Unclamped Inductive Switching Circuit & Waveforms

Package Mechanical Data-PDFN5060-8L(CLIP)- Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070